

**Amendments to the Drawings:**

All of the following changes are implemented on the attached replacement sheets and shown on the annotated sheets attached following page 24 of this paper:

In Figure 7, block 603 is relabeled as --INTF IN--;

In Figure 13, the signal line "Serial Out" is relabeled as --1253-- and is now pointing toward block 1150;

In Figure 17A, floating gates have been added to the transistors in 1400 and 1420;

In Figure 17B, the control gate of 1465 has been relabeled --CLK K--;

In Figure 21B, the block for  $\Delta I_2$  is relabeled as --1453--; and

In Figure 22, the memory cells 1 to n have had floating gates added.

## REMARKS

This is in response to the Office Communication mailed on mailed on July 12, 2006, and for which a one-month extension is requested.

### Objections to the Drawings

The Office Action raised a number of objections to the drawings. A number of corrections have been made, as described above and shown in the accompanying sheets. A number of the noted objections are, however, believed to be in error and aside from the changes being currently made, it is respectfully submitted that the drawings previously submitted on December 18, 2003, are otherwise accurate, consistent, and acceptable. If the Examiner has any questions on specific objections, a call to the undersigned is requested.

### Objections to the Specification

The Office Action raised a number of objections to the specification. These have all been attended to as noted above, with the exception of the objection raised with respect to page 6, line 17, where it is believed that the specification is correct in its current form.

### Double Patenting Rejection

The Office Action gave an obviousness-type double patenting rejection to claims 63-91 based on US patent 5,991,517, which is the parent of the present application. Although the validity of this rejection has not been considered in detail and thus no conclusion has been reached as to the whether the rejection is well taken or not, a terminal disclaimer is being filed with the present response in order to facilitate the application process.

### Rejections under 35 USC § 102

The Office Action has rejected claims 63-91 under 35 U.S.C. §102(b) as being unpatentable over the prior art. It is respectfully submitted that this rejection is improper and should be withdrawn. As noted in the Preliminary Amendment that was filed concurrently with the present application, independent claims 63-91 are respectively exact copies of claims 1-17 and 43-54 of U.S. patent number 5,657,270 of Ohuchi *et al.*. The grounds of rejection of claims 63-91 of the present application are ones that would also be equally applicable to claims 1-17

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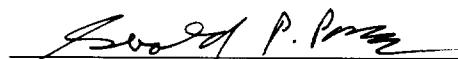
Attorney Docket No.: SNDK.006USS

Application No.: 09/129,675

and 43-54 of U.S. patent number 5,657,270. Consequently, the Office Action is holding as unpatentable claims 63-91, which are copied from U.S. patent number 5,657,270 for interference purposes, relying upon grounds that are equally applicable to U.S. patent number 5,657,270. As such, the rejection is improper and should be withdrawn.

In particular, the Examiner is referred to item 6 of section 1003 of the M.P.E.P. that lists matters that are to be submitted to the Technology Center Directors. As stated there, these matters include: "6. Actions which hold unpatentable claims copied from a patent for interference purposes where the grounds relied upon are equally applicable to the patentee". As discussed in the preceding paragraph above, this is the case of the prior art rejection given in the Office Action; therefore, the rejection must have the approval of the TC Director. Since the Office Action in the present application has not provided this special approval, the rejection is consequently improper and should therefore be withdrawn.

Respectfully submitted,



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10/25/06  
Date

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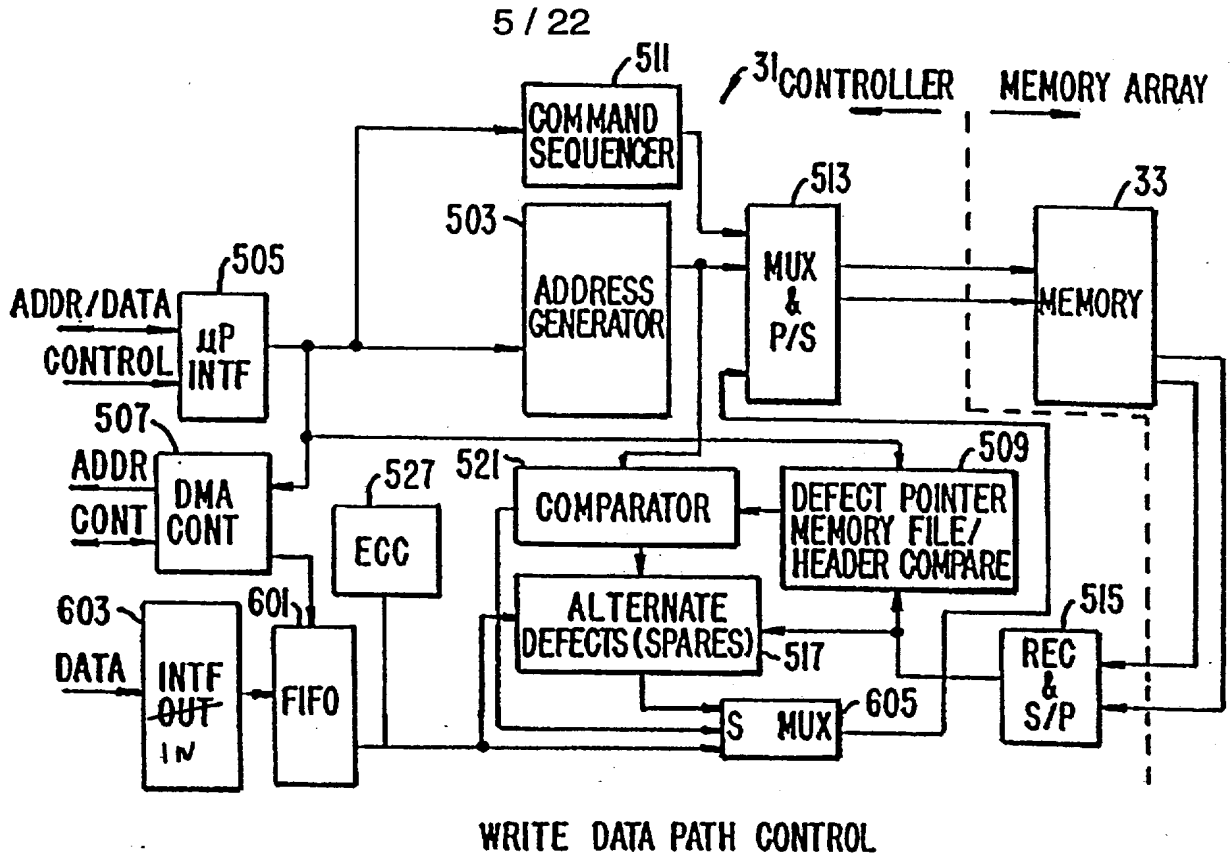
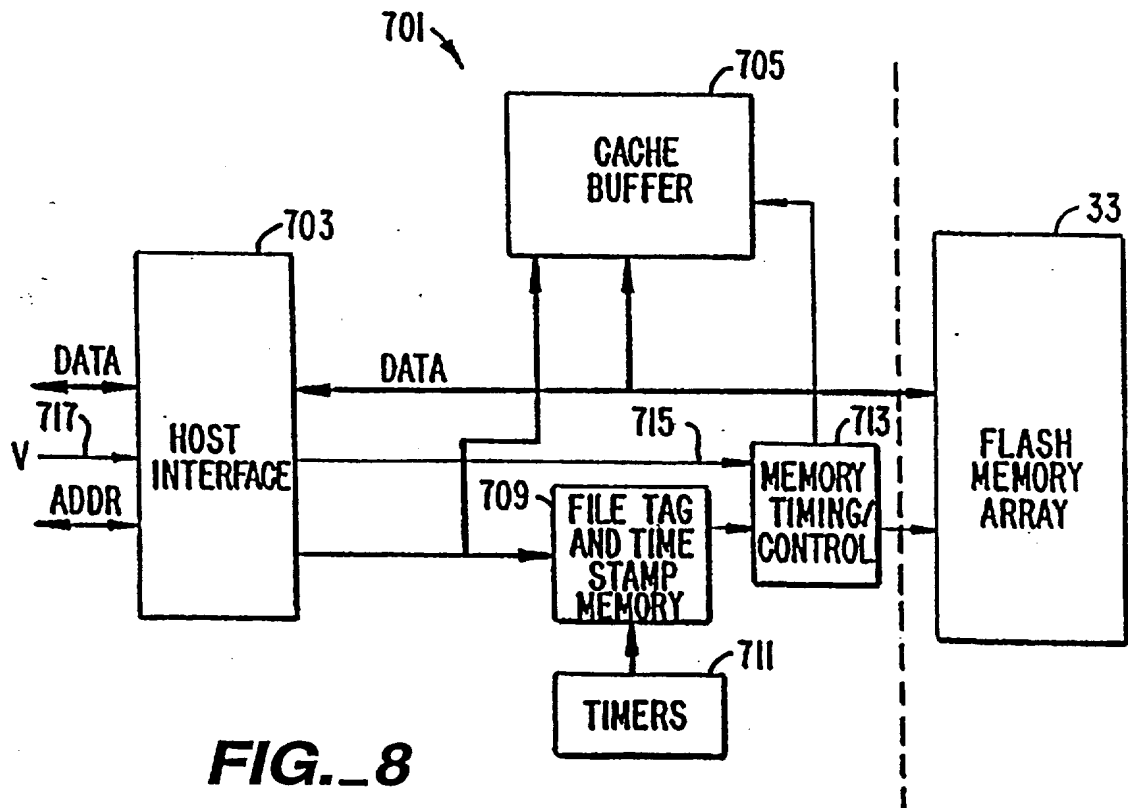


FIG. 7



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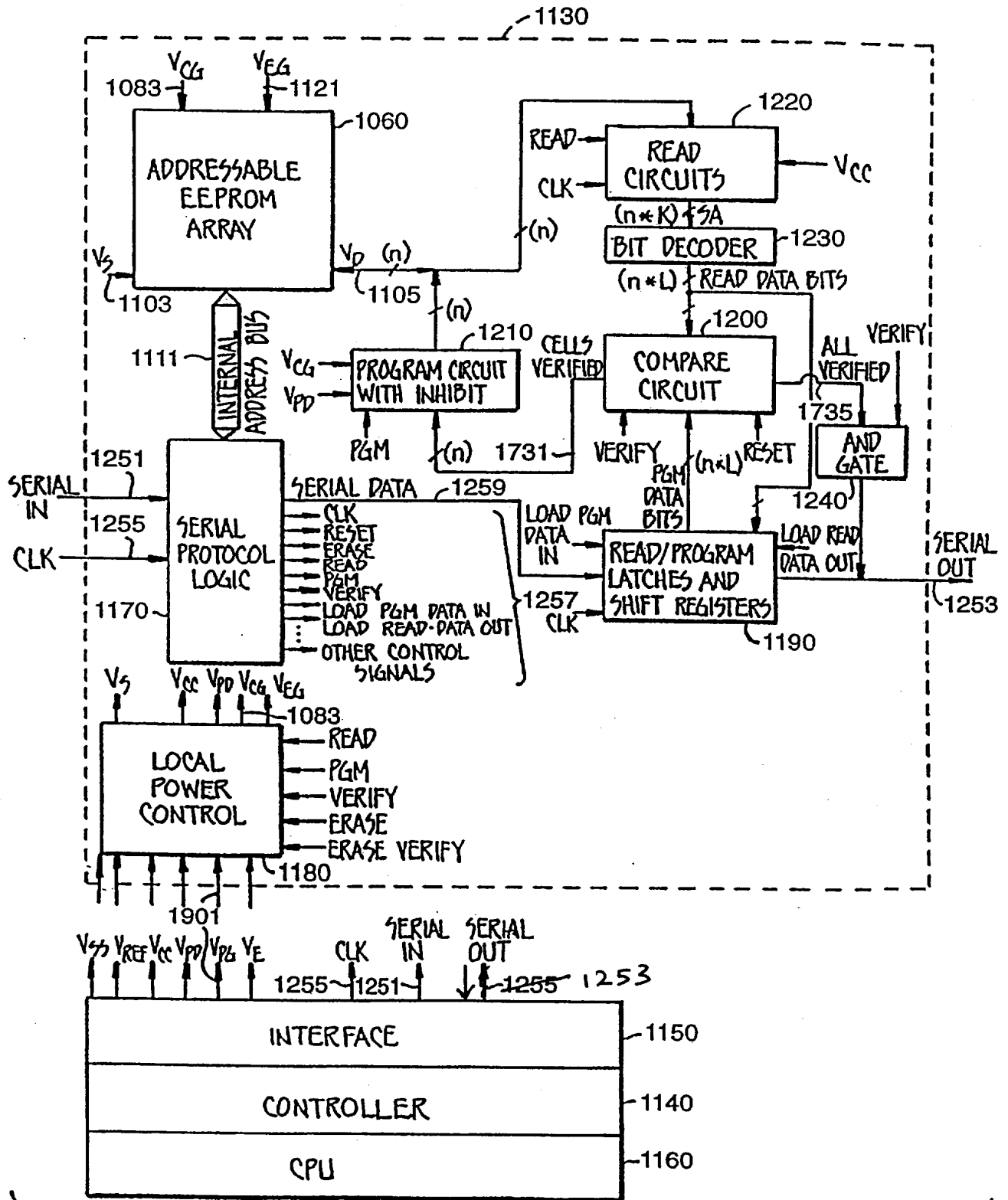
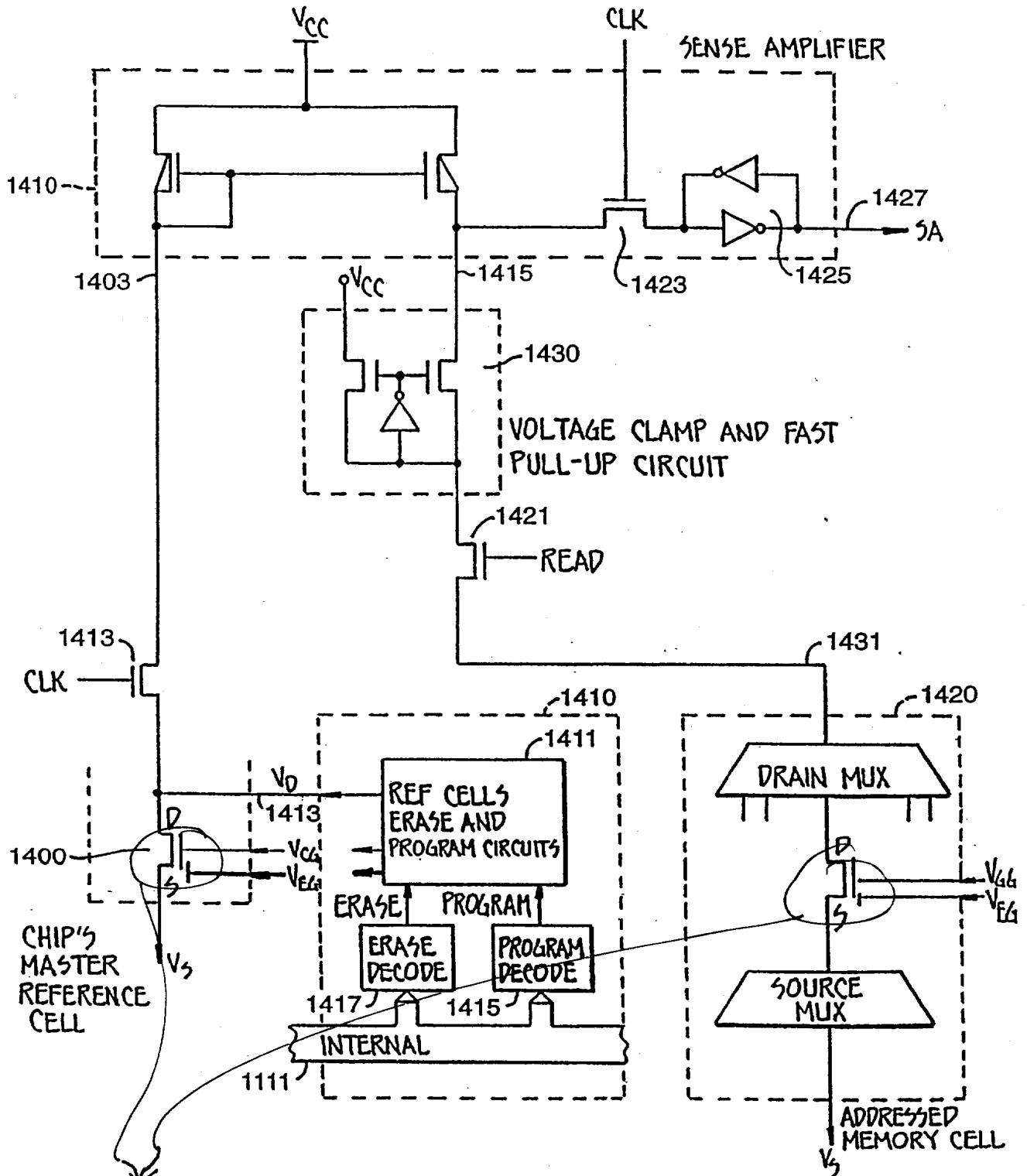


FIG. 13

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for both, replace with

**FIG. 17A**



where the 1 is added

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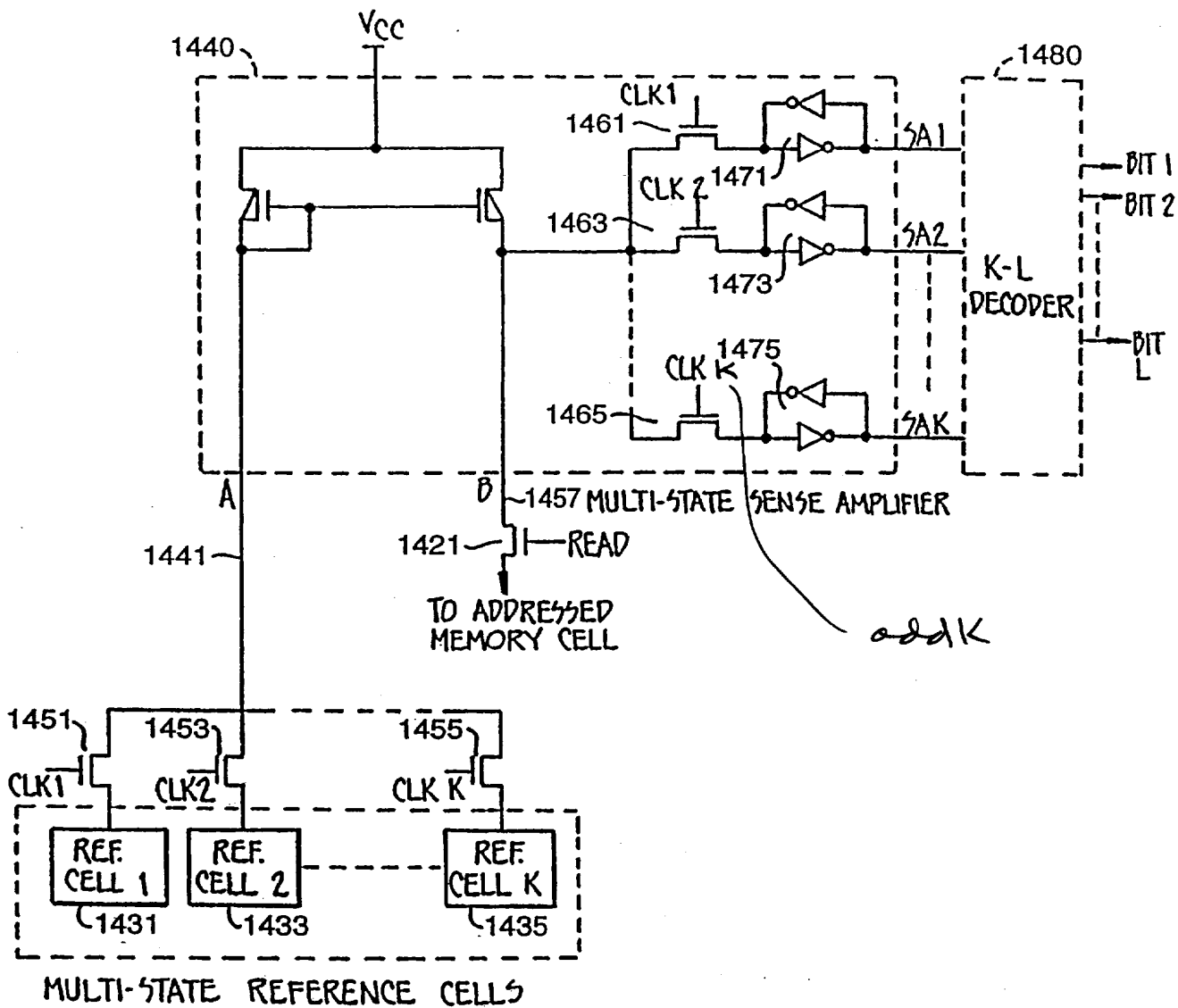
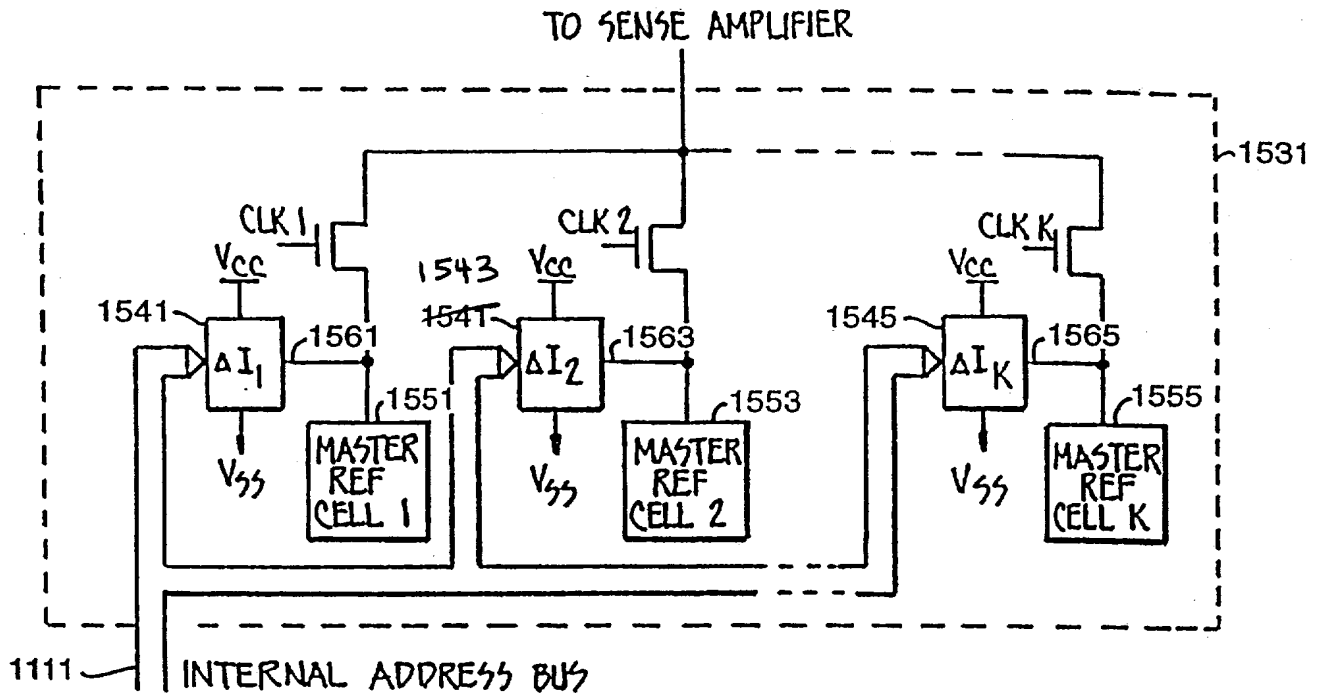
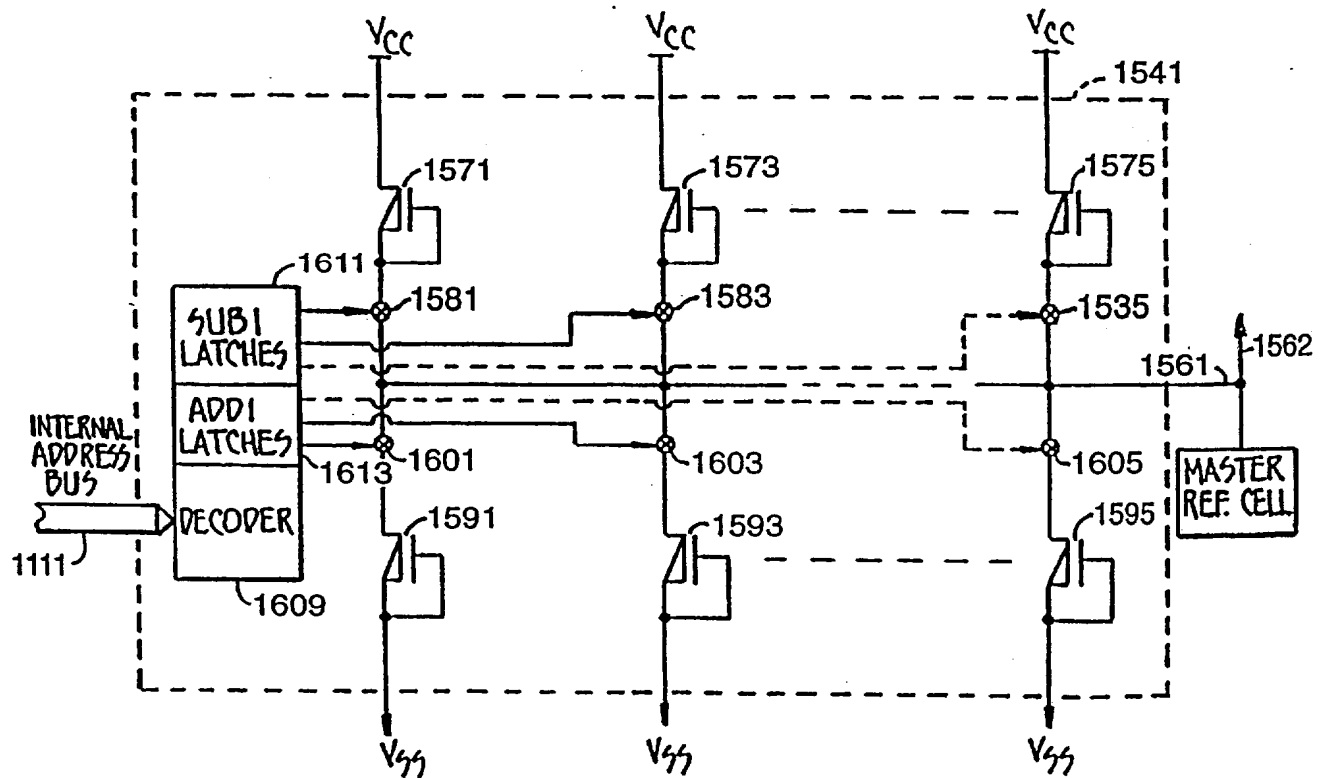


FIG. 17B

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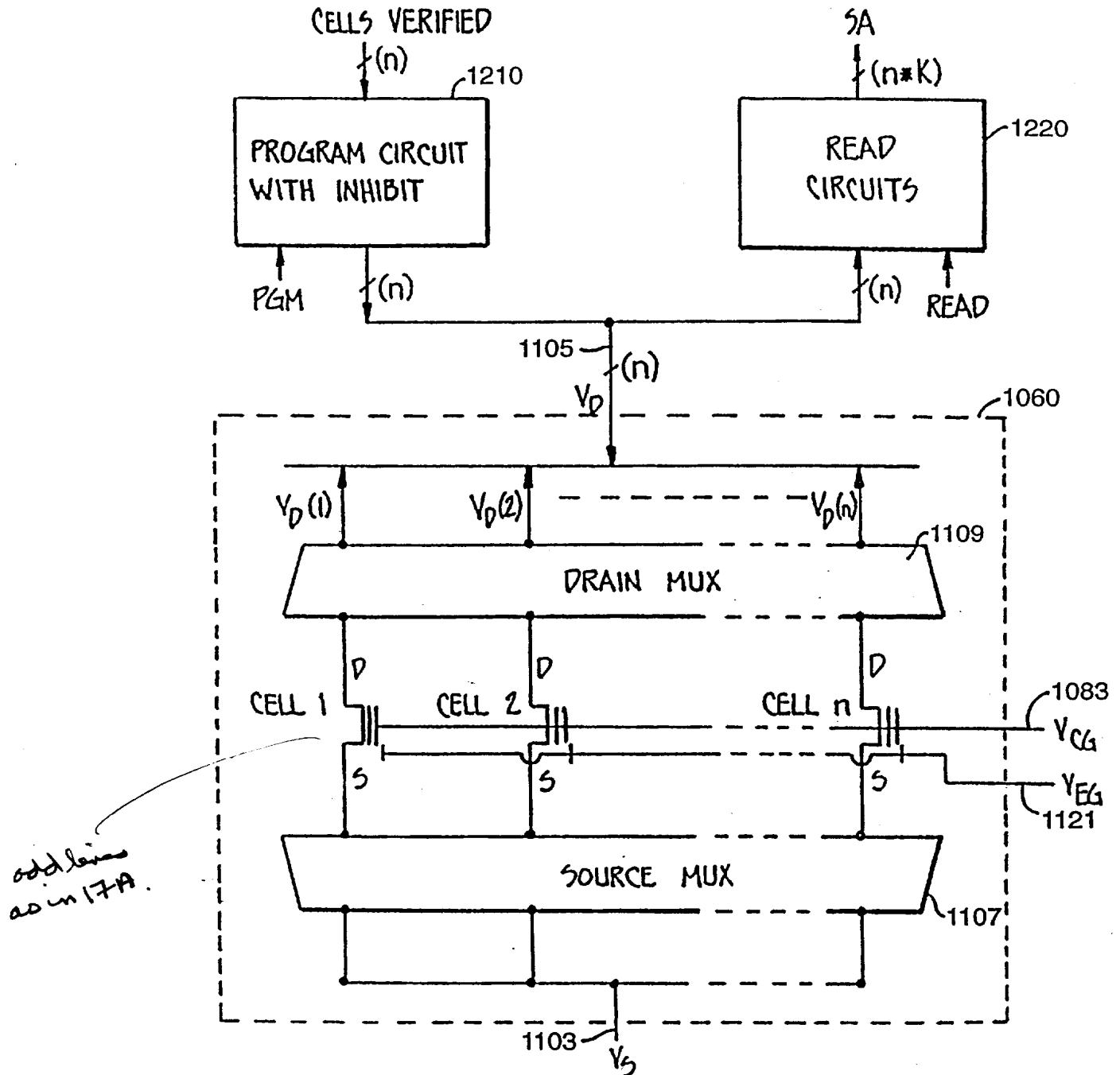


**FIG. 21B**



**FIG. 21C**

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READ/PROGRAM DATA PATHS FOR  $n$  CELLS IN PARALLEL

**FIG. 22**